

## **Annual Report**

Unclonable RFID-based Tag-Seal for Storage Containers

Project number SL11-UnclonRFID-PD12

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## Unclonable RFID-based Tag-Seal for Storage Containers

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Per the LCP, our task in this no cost extension year is the following:

“In the final year, we will execute accelerated aging of integrated circuit PUFs to assess long term reliability of PUF outputs and report on the results.”

Our accomplishments:

### Established a Test Plan

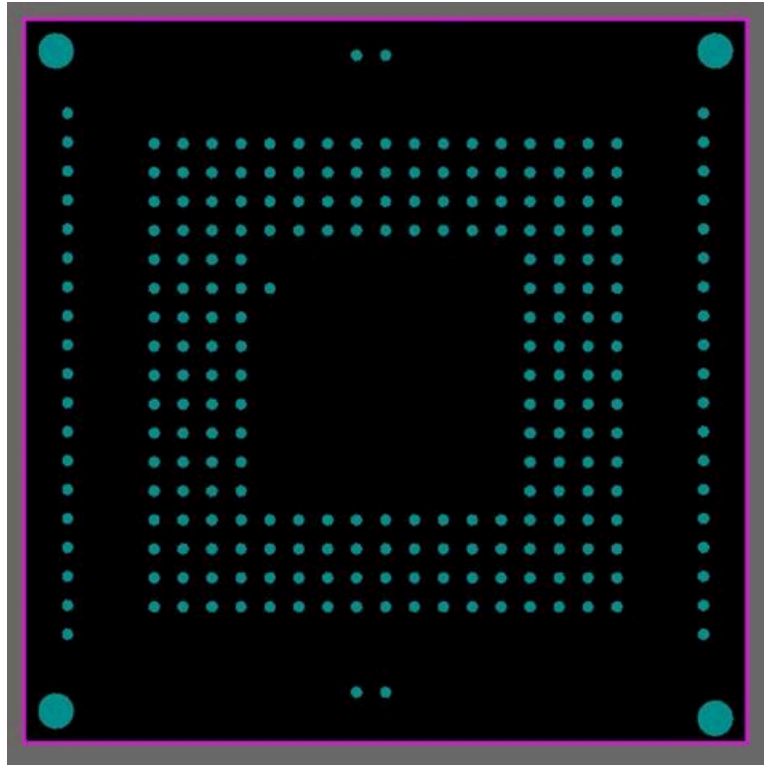
We are using the DoD MIL-STD as our guide for microelectronics aging (MIL-STD 883J, Method 1016.2: Life/Reliability Characterization Tests). In that document they recommend aging at 3 temperatures between 200-300C, separated by at least 25C, with the supply voltage at the maximum recommended voltage for the devices at 125C (3.6V in our case). If that voltage causes excessive current or power then it can be reduced and the duration of the tests extended. The MIL-STD also recommends current limiting resistors in series with the supply. Since we don't have much time and we may not have enough ovens and other equipment, two temperatures separated by at least 50C would be an acceptable backup plan.

To ensure a safe range of conditions is used, we are executing 24-hour step tests. For these, we will apply the stress for 24 hours and then measure the device to make sure it wasn't damaged. During the stress the PUFs should be exercised, but we don't need to measure their response. Rather, at set intervals our devices should be returned to nominal temperature (under bias), and then measured. The MIL-STD puts these intervals at 4, 8, 16, 32, 64, 128, 256, 512 and 1000 hours, although the test can be stopped early if 75% of the devices have failed.

A final recommendation per the MIL-STD is that at least 40 devices should be measured under each condition. Since we only have 25 parts, we will place 10 devices in each of two stress conditions.

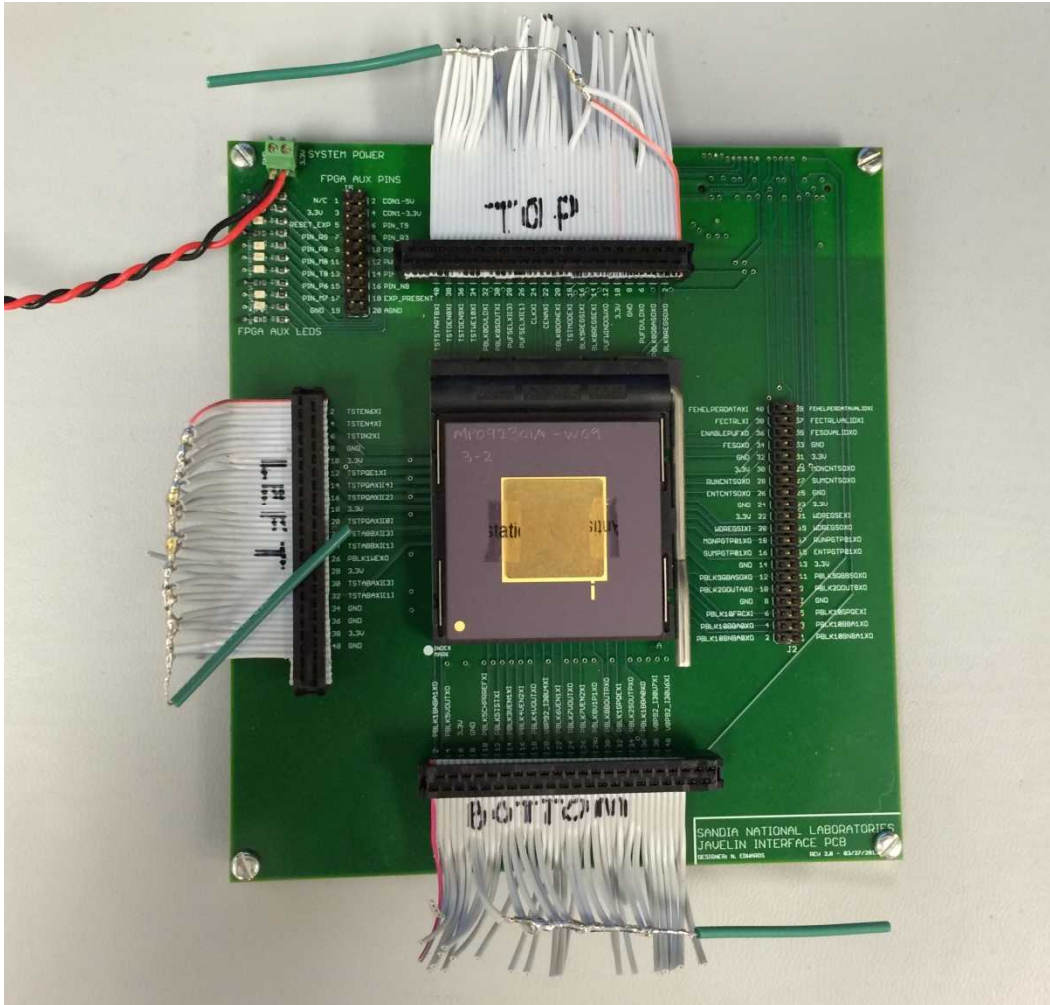
### Designed and Procured Custom Printed Circuit Boards and Associated Components

Because we need to have our PUF circuits powered on during the high stress condition, we designed and procured a new PCB that will allow us to do so. A screen capture of a portion of the PCB design is shown below. We will test the integrated circuit PUF on previously existing infrastructure. This PCB is just to allow us to power the circuits during the stress condition. We also procured the components to populate the board.



### Printed Circuit Board Assembly

We assembled five boards. Our initial evaluation of the boards showed that the low insertion force socket for our integrated circuit (IC) package requires too much force to insert reliably by hand, with the risk being damaged pins on our valuable ICs. To mitigate the risk, we designed and fabricated a small tool to aid in the insertion, and we do the insertion on a mechanical press to ensure that the insertion force is normal to the surface so we don't bend pins. Printed circuit board assembly was an unexpected challenge and resulted in a many month time delay for us.



## Test Program Troubleshooting

Testing of one of our threshold voltage PUF circuits in preparation for reliability testing indicated poor inter-device variation at low supply voltage. Initially we established two models that could lead to the response but we were able to verify that neither model was sufficient to explain all of the data. After more troubleshooting we confirmed that, at low supply voltage, we inadvertently pulled a specific test pin high, which diverted enough power that power to our PUF was unbalanced and we had a dominant circuit in our PUF circuit pairs at low voltage as a consequence.

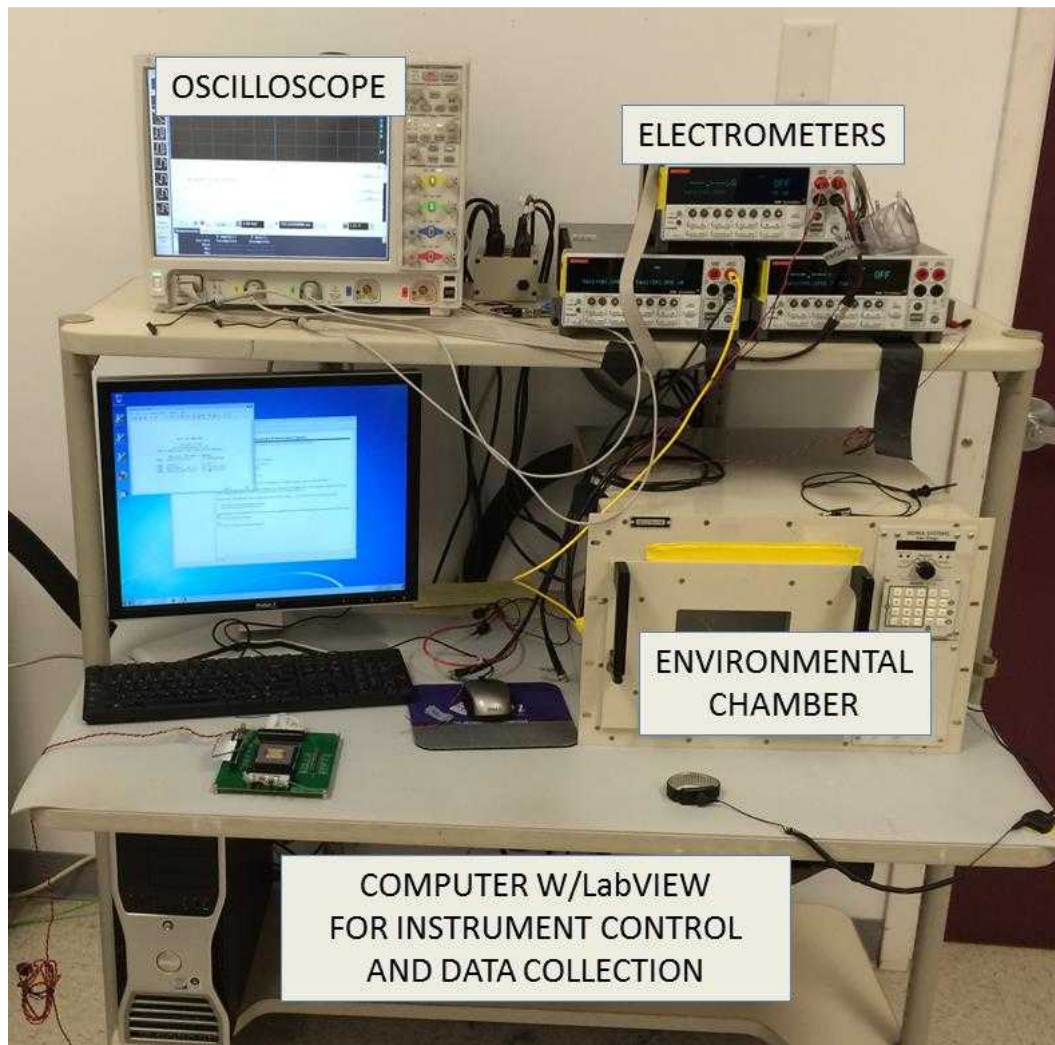
## Fact Sheet

We wrote and iterated on a fact sheet this year.

## Test Apparatus Optimization

Typically we test only one PUF at a time but for reliability testing, since it takes a long time even under accelerated aging conditions to assess reliability, we configured our test

apparatus to support five integrated circuits at time. This required additional electrometers to power the additional integrated circuits as well as modifications to our instrument control.



#### Comments:

We failed to complete our task this year primarily due to unexpected difficulty assembling the printed circuits boards that enable us to power the integrated circuits during the accelerated aging conditions. In late December we lost the technologist that we expected to work on this project and there was loss of continuity due to that. However, our test apparatus is now assembled and our LabVIEW virtual instrument for instrument control and data collection is functional, so we do expect to execute reliability tests on other funding in the future. We did also successfully troubleshoot an integrated circuit test problem that artificially suppressed our PUF performance metrics. In total we spent about \$11k this FY.